

High Performance Multi-Channel Time Interval Counter with Integrated GPS Receiver

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Abstract

A new time interval counter has been developed for PC-based time and frequency measurement applications. The counter incorporates a multi-channel design, allowing concurrent measurements of up to 11 input signals. Each input signal can be compared to a reference oscillator or to the signal from an integrated GPS receiver. Other features include 24-bit programmable dividers that allow the measurement of any frequency from 1 Hz to 167.77 MHz, single shot resolution of < 30 ps and an Allan deviation $[\sigma_y(\tau)]$ of **2.5×10^{-14} at $\tau = 1024$ s** during a self test. A discussion of the counter design, the theory of operation, measurement performance, and potential applications in time and frequency metrology is included.

Introduction

Time interval measurements are significant in the characterization of oscillators. To perform both short-term and long-term measurements, a time interval counter should be designed to optimize resolution and stability. Multi-channel capabilities allow a counter to simultaneously compare several oscillators to a reference oscillator. Integrating a GPS receiver adds the option of using its composite frequency or an individual satellite frequency as an additional reference oscillator. Using such features, high level calibrations can be performed over short or long term intervals. By implementing a counter on a PC card, data can be continuously collected, analyzed, stored and displayed by the PC. A new counter card has been designed to utilize these characteristics and improve upon previous designs.

Counter Design

The Multi-Channel Time Interval Counter (MCTIC) is a computer card measuring 114 x 229 mm, and it was designed to work with any PC that supports the Industry Standard Architecture (ISA) expansion bus. A commercially-available Global Positioning System (GPS) satellite receiver plugs directly into a 10-pin connector mounted on the card. This allows the counter software to control the GPS receiver as well as utilize its outputs. The receiver dimensions are 50.8 x 82.6 x 16.3 mm.

The MCTIC resides in memory at either 200h or 300h (jumper selectable) and occupies 32 bytes of I/O address space. All functions (other than the base address selection) are configurable in software. The counter includes an inexpensive 10 MHz crystal as a time base oscillator but, for the best measurement results, an external oscillator should be used as its reference.

Nine sub-miniature (SMB) connectors are mounted along the edge of the MCTIC. The first eight connectors are input channels which can accept either sinusoidal or TTL signals. Each input passes through a programmable divide-by-10 prescaler and a 24-bit divider, either of which can be bypassed if necessary. This allows any input frequency from 1 Hz to 167.77 MHz to be used for 1 pps time interval measurements. Other suitable low frequencies (10 pps or 100 pps, for example) can also be used as the measurement rate by changing the divider settings. The last SMB connector accepts 1, 5 or 10 MHz as the external reference frequency for the time base. There are three additional channels with no dividers for low frequency signal inputs (TTL only).

The eight input signals are passed through a multiplexer and, in sequence, each one is selected as either the start or stop input to the counter and compared against the time base or one of the three non-divided input channels (Figure 1). The start and stop combinations are set independently for each channel in software.

The GPS receiver can simultaneously track eight satellites and is software controlled using an RS-232 interface included in the MCTIC circuitry. The output timing frequency from the GPS receiver, either 1 pps or 100 pps, is directly connected to one of the non-divided input channels.

The majority of the counter's digital circuitry is included in a *programmable logic device* (PLD) chip. The PLD is programmed by loading a binary file from the PC, and provides two major advantages over discrete components. First, it allows changes to be made to the MCTIC circuitry without physically changing any of the on-board components. Second, it allows measurement noise and delays to be kept to a minimum since all of the counter and divider circuitry is housed in a single integrated circuit.

Theory of Operation

The MCTIC uses three counters to produce time interval readings: the main counter, the start interpolator counter and the stop interpolator counter. The main counter provides the MCTIC with its coarse resolution (100 ns), and the start and stop interpolator counters provide the MCTIC with its fine resolution (< 30 ps).

The main counter is a 24-bit device that counts the zero crossings of the 10 MHz time base frequency. It begins counting zero crossings when a start pulse is received and stops counting zero crossings when a stop pulse is received. The resolution of the main counter is limited to the period of 10 MHz (100 ns). The values read from the 16-bit start and stop counters are used to interpolate the time intervals between zero crossings. The interpolation scheme uses analog circuitry and has been previously described in detail by Zhang [1].

The interpolation scheme determines where the start and stop pulses lie between the time base zero crossings. The start counter measures the time interval between the start pulse and the first

zero crossing from the time base. The stop counter measures the interval between the last zero crossing from the time base and the stop pulse.

In order for the interpolation scheme to work, the MCTIC is calibrated using a two-part software algorithm. First, the start and stop counters are calibrated using a reference voltage obtained by charging and discharging two ramping capacitors. The counters are observed during a 100 ns interval, and the software records the minimum and maximum counter values during this interval. The resolution of each counter can be determined by dividing 100 ns by the range of counter values (maximum – minimum). For example, 100 ns / 4000 counts equals 25 ps resolution. The second part of the calibration determines the path delay in the counter circuitry. The delay measurement is made by dividing the 10 MHz time base frequency by 256 to obtain a frequency of 39062.5 Hz and then supplying this frequency to both the start and stop inputs of the counter. The period of this frequency is 25600 ns. A number of time interval measurements are made, and the variation from the expected answer is computed. This variation indicates the counter delay.

When the counter is calibrated, five values are obtained: the maximum values of the start and stop counters (ST_{\max} and SP_{\max}), the minimum values of the start and stop counters (ST_{\min} and SP_{\min}) and the counter delay (D). When the counter is read, three values are obtained: the main counter reading (N_{main}), the start counter reading (N_{start}) and the stop counter reading (N_{stop}). T represents the period of the counter's time base frequency. The equation below illustrates how the time interval reading, Δt , is derived using these values:

$$\Delta t = N_{\text{main}}T + \frac{N_{\text{start}}T}{ST_{\max} - ST_{\min}} - \frac{N_{\text{stop}}T}{SP_{\max} - SP_{\min}} - D$$

Measurement Results

Figure 2 shows the measurement configuration for a 1 pps self-test. A 1 pps signal from a cesium oscillator is used for both the start and the stop pulses, with an additional section of cable inserted before the stop channel to introduce a fixed delay.

Figure 3 is a phase plot of a 200000 s measurement run. Nearly all of the readings fall within a band of about 55 ps (double the counter resolution) indicating an error of plus or minus one count centered around a count of 160.45 ns (the cable delay). An analysis of the data (Figure 3) shows an Allan deviation $[\sigma_y(\tau)]$ of **8×10^{-16} at $\tau = 32768$ s** and that the MCTIC has yet to reach its noise floor. A time deviation plot $[\sigma_x(\tau)]$ shows stability of better than **1 ps at $\tau = 1024$** and a flicker floor of **6×10^{-13} , $\tau = 16384$ s** (Figure 4).

The self-test data suggest that the MCTIC is well suited for the calibration and characterization of oscillators over both long and short term intervals.

Applications

The MCTIC was specifically designed for use with the NIST Frequency Measurement and Analysis Service (FMAS). This service allows a customer to obtain a measurement system from NIST for installation in his/her laboratory. The measurement system continually measures each of the customer's frequency standards against a GPS signal that is also being monitored at the NIST laboratories in Boulder, Colorado. Continuous measurements are made and logged in the PC while displaying current counts, hourly averages and graphs of frequency offset for each input channel. NIST personnel then download the customer's measurement data and send a monthly calibration report. The report includes a statement of measurement uncertainty and establishes traceability to the United States national frequency standard [2,3].

Another potential application of the MCTIC is its use as a common-view GPS receiver. The onboard receiver is a multi-channel device that allows individual satellite data to be extracted so common-view tracks can be logged. Work on a multi-channel common-view device utilizing the MCTIC is in progress at NIST.

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References

- [1] V.S. Zhang, D. D. Davis and M.A. Lombardi, "High Resolution Time Interval Counter," in *Proc. 26th Annual Precise Time and Time Interval Meeting (PTTI)*, 1994, pp. 191-200.
- [2] M. A. Lombardi, "NIST Frequency Measurement Service," *Cal Lab: The International Journal of Metrology*, May-June 1995, pp. 11-17.
- [3] M. A. Lombardi, "Automation of NIST Frequency Calibrations at Remote Sites," in *Proc. IEEE Instrumentation and Measurement Technology Conference*, Venice, Italy, May 1999, pp. 618-622.

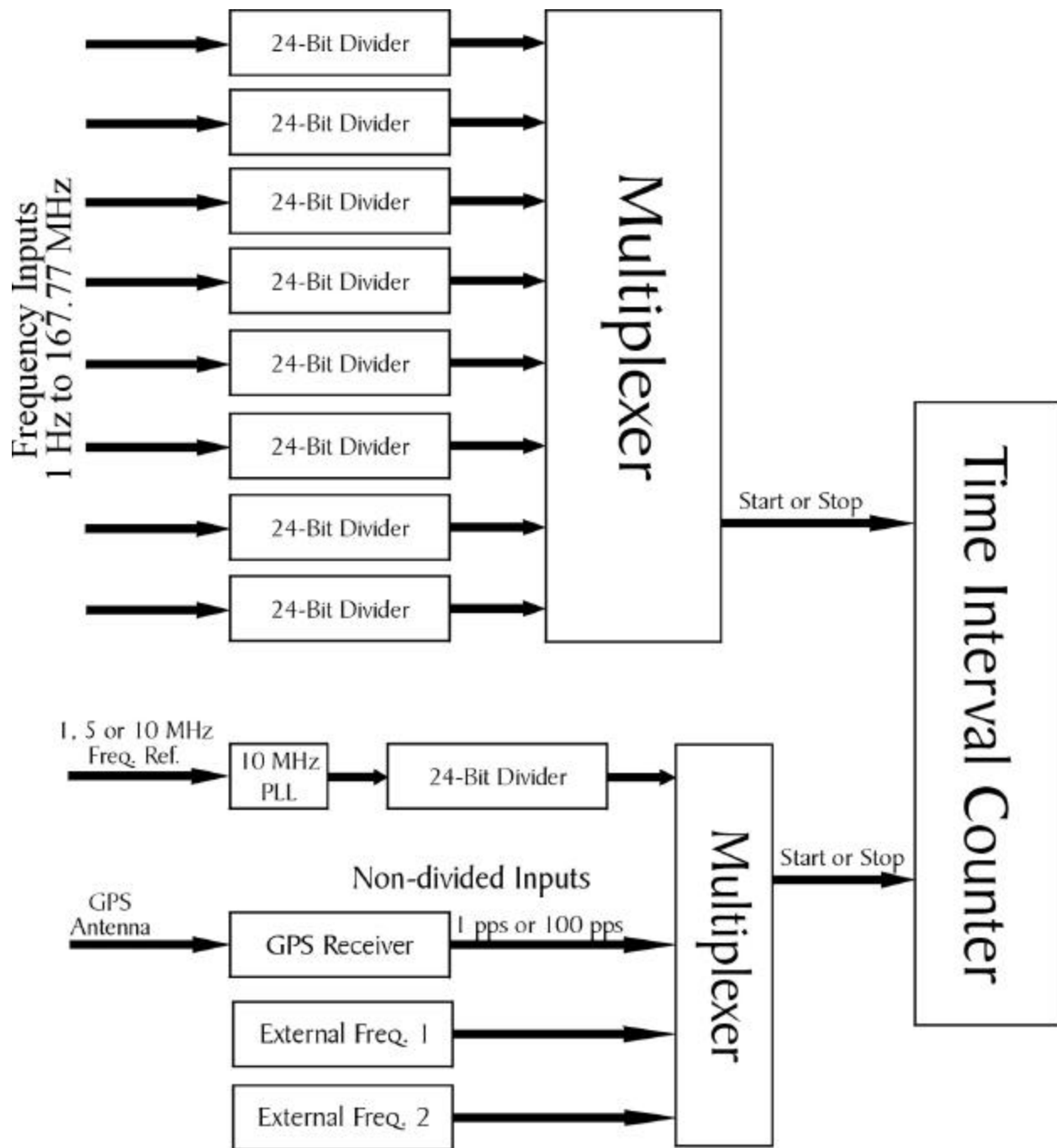


Figure 1. Block Diagram of MCTIC

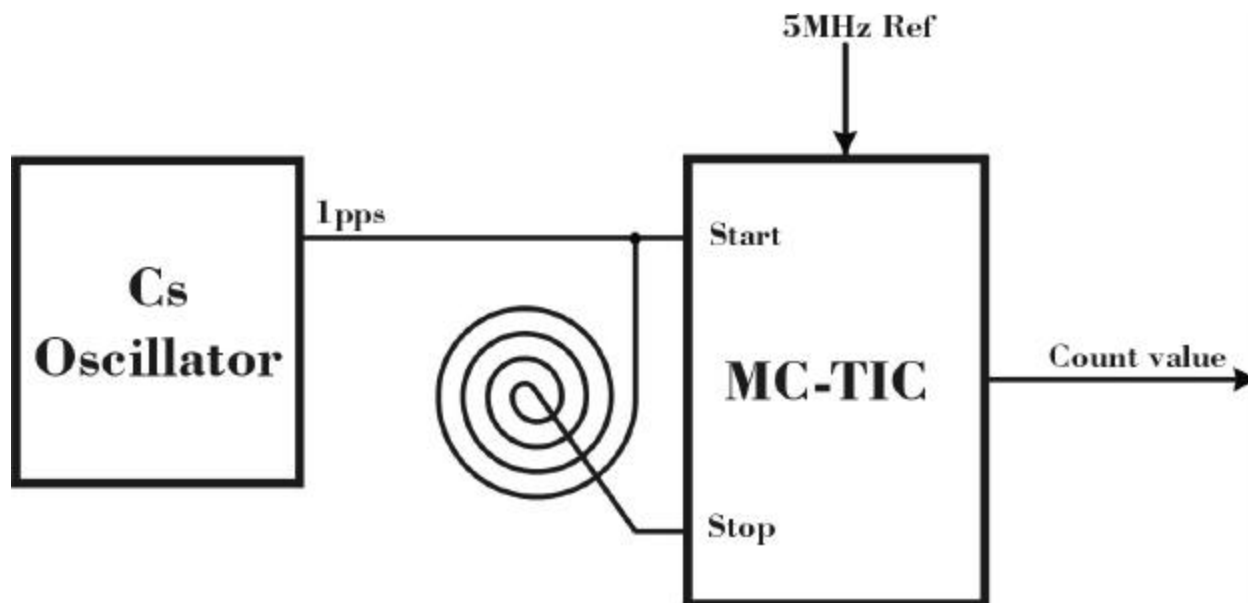


Figure 2. 1 pps Self Test Startup

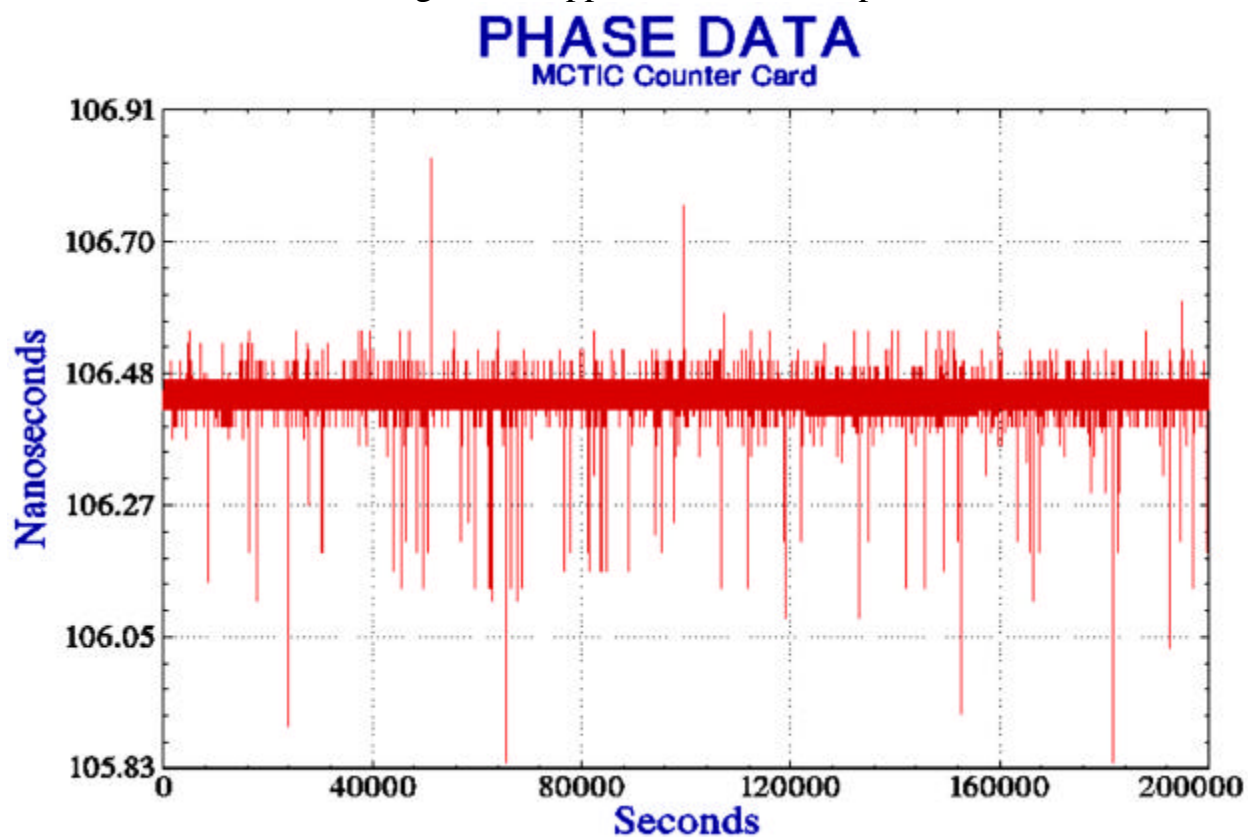


Figure 3. Phase Plot of Self Test Data

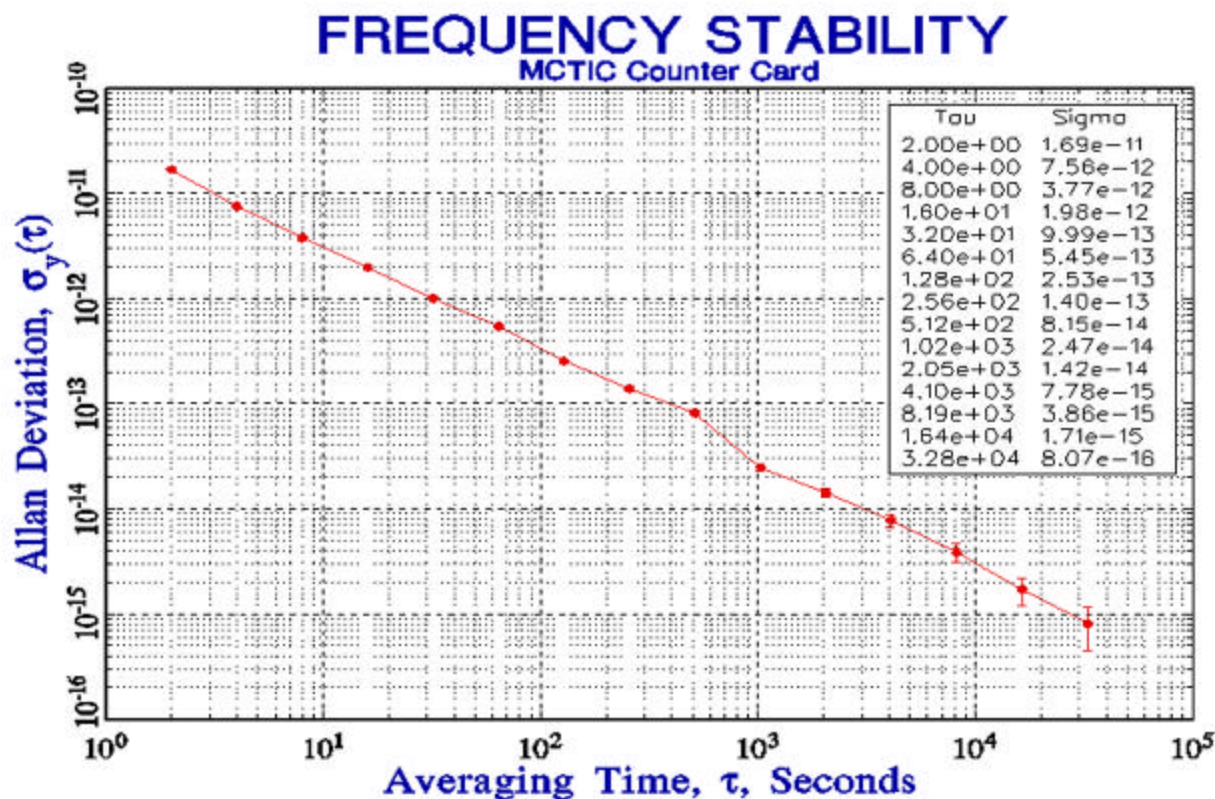


Figure 4. Allan deviation of Self Test Data

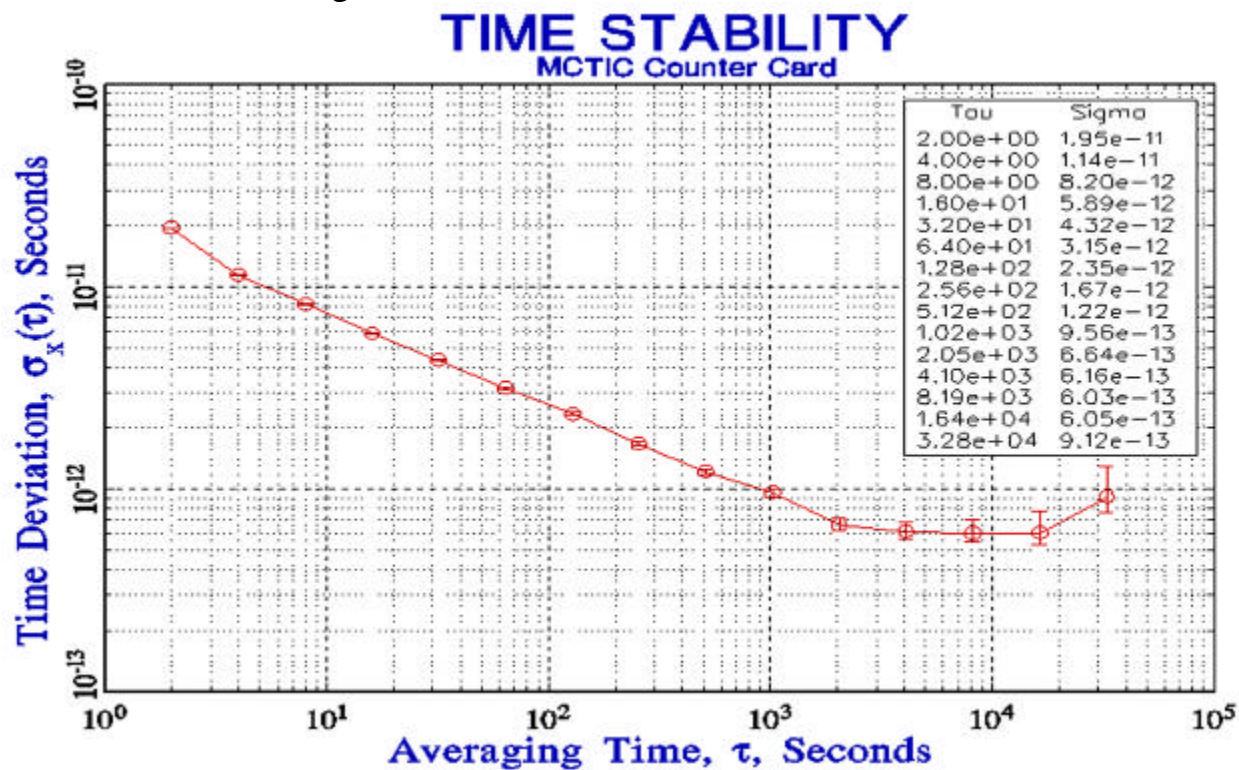


Figure 5. Time deviation of Self Test Data